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**UTILITY  
PATENT APPLICATION  
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Attorney Docket No. 042390.P6349

First Inventor or Application Identifier Rajeev K. Nalawadi

Title 82C59 Redirection to I/O APIC

Express Mail Label No. EM560890943US

**APPLICATION ELEMENTS**

See MPEP chapter 600 concerning utility patent application contents

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 - Cross References to Related Applications  
 - Statement Regarding Fed sponsored R & D  
 - Reference to Microfiche Appendix  
 - Background of the Invention  
 - Brief Summary of the Invention  
 - Brief Description of the Drawings (if filed)  
 - Detailed Description  
 - Claim(s)  
 - Abstract of the Disclosure
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4. Oath or Declaration Total Pages
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7.  Assignment Papers (cover sheet & document(s))
8.  37 CFR 3.73(b) Statement  Power of Attorney  
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9.  English Translation Document (if applicable)
10.  Information Disclosure Statement (IDS)/PTO - 1449  Copies of IDS Citations
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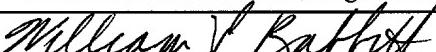
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Attorney's Docket No. 042390.P6349  
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UNITED STATES PATENT APPLICATION

FOR

**82C59 REDIRECTION TO I/O APIC**

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## 82C59 REDIRECTION TO I/O APIC

### BACKGROUND OF THE INVENTION

#### 5 Field of the Invention

The invention relates to computer system peripheral connections and more particularly to managing system interrupts.

#### Background

10 Peripheral Component Interconnect (PCI)-Extended Industry Standard Architecture (EISA) bridge sets provide an I/O subsystem for many computer systems. One Peripheral Component Interconnect (PCI) standard is PCI Local Bus standard version 2.2 (January 5, 1999). The chip set generally consists of two components--the PCI-EISA Bridge (PCEB) and the EISA system component (ESC). In general, the ESC implements system functions such as timer-counter, direct memory access (DMA), and interrupt control.

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In one form of interrupt control utilized in certain chip set configurations of Intel Corporation of Santa Clara, California, an EISA compatible interrupt controller of the ESC incorporates the functionality of two 82C59 interrupt controllers that are cascaded providing fourteen external and two internal interrupts. The ESC also contains an Advanced

Programmable Interrupt Controller (APIC). The APIC can be used in either a uni-processor or multi-processor system. The APIC provides multi-processor interrupt management and incorporates both static and dynamic symmetric interrupt distribution across all processors. In systems with multiple I/O subsystems, each system can have its own set of interrupts.

As noted, the EISA compatible interrupt controller incorporates the functionality of two 82C59 interrupt controllers. The two controllers are cascaded into a master interrupter controller and a slave interrupt controller. Two internal interrupts are used for internal function only and are not available at the chip periphery. One interrupt is used to cascade the two controllers together and another is used as a system timer interrupt. The remaining 14 interrupt lines are available for external system interrupts. The interrupts are programmed to utilize on the order of 2000 logic gates.

Examples of uses of the 14 system interrupts include interrupts for a keyboard, hard drive, modem, etc.

While the standard EISA compatible interrupt controller is intended for use in a uni-processor system, the APIC can be used in either a uni-processor or multi-processor system. An APIC provides multi-processor interrupt management and incorporates static and dynamic symmetric interrupt distribution across all

processors. In systems with multiple I/O subsystems, each subsystem can have its own set of interrupts.

At the system level, an APIC consists of two parts--one residing in the I/O subsystem (I/O APIC) and the other in the 5 CPU (local APIC). The ESC contains the I/O APIC unit.

The I/O APIC unit consists of a set of interrupt input signals, a 16-entry Interrupt Redirection Table, programmable registers, and a message unit for sending and receiving APIC messages over the APIC bus. I/O devices inject interrupts into 10 the system by asserting one of the interrupt lines to the I/O APIC. The I/O APIC selects a corresponding entry in the redirection table and uses the information of that entry to format an interrupt request message. Each entry in the redirection table can be individually programmed to indicate 15 edge/level sensitive interrupt signals, the interrupt vector and priority, the destination processor, and how the processor is selected (e.g., statically or dynamically). The information in the table is used to transmit a message to other APIC units via the APIC bus.

20 In addition to its compatibility with multi-processor environments, the APIC system offers the ability to handle a greater number of system interrupts with greater flexibility than the EISA compatible interrupt controller. Nevertheless, the EISA compatible interrupt controller remains a legacy

standard for interrupt control in the modern processor environment.

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SUMMARY OF THE INVENTION

In one aspect, a method is disclosed. The method includes trapping initializing data of a first interrupt type to a first interrupt controller. The initializing data of the first interrupt type is re-routed to a second interrupt controller. The second interrupt controller is configured to manage interrupts of the first interrupt type.

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Wm. Wm. Wm. Wm. Wm. Wm. Wm.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The features, aspects, and advantages of the invention will become more thoroughly apparent from the following detailed description, appended claims, and accompanying drawings in which:

**Figure 1** is a schematic block diagram of a multi-processor environment illustrating the interrupt control for the system.

**Figure 2** is a flow chart of an embodiment of the method of the invention.

**Figure 3** is a specific embodiment of the method of the invention.

DETAILED DESCRIPTION OF THE INVENTION

In one aspect, the invention relates to a method and system to handle all system interrupts through the APIC system, including processor systems that rely for at least a portion of 5 their interrupt control on the legacy standard of the EISA compatible interrupt controller. In this manner, the invention allows systems that rely partially on EISA compatible interrupt controllers, such as the 82C59 interrupt controller to be incorporated in a multi-processor environment. By utilizing the 10 APIC system of interrupt control the number of dedicated gates required for interrupt control can be reduced.

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**Figure 1** schematically illustrates a block diagram of a multi-processor environment suitable for interrupt control according to the invention. System 100 is a multi-processor system, including processor 110, processor 210, and processor 310. Each processor contains a memory element (e.g., random access memory, read only memory, cache, etc.) System 100 also includes, in this illustration, EISA system component (ESC) 410. ESC 410 incorporates the standard EISA compatible interrupt controller and the APIC. In one embodiment, the EISA compatible interrupt controller includes two 82C59 interrupt controllers arranged in a master (CNTRL-1)-slave (CNTRL-2) configuration as known in the art. In one embodiment, the two 82C59 interrupt

controllers are utilized to control the interrupt functions listed in Table 1:

Table 1: Typical Interrupt Functions

| Priority | Label | Controller | Typical Interrupt Source                          |
|----------|-------|------------|---|
| 1        | IRQ0  | 1          | Interval Timer 1, Counter 0 OUT                   |
| 2        | IRQ1  | 1          | Keyboard  |
| 3-10     | IRQ2  | 1          | Interrupt from Controller 2                       |
| 3        | IRQ8# | 2          | Real Time Clock                                   |
| 4        | IRQ9  | 2          | Expansion Bus Pin B04                             |
| 5        | IRQ10 | 2          | Expansion Bus Pin D03                             |
| 6        | IRQ11 | 2          | Expansion Bus Pin D04                             |
| 7        | IRQ12 | 2          | Expansion Bus Pin D05                             |
| 8        | IRQ13 | 2          | Coprocessor Error, Chaining                       |
| 9        | IRQ14 | 2          | Fixed Disk Drive Controller Expansion Bus Pin D07 |
| 10       | IRQ15 | 2          | Expansion Bus Pin D06                             |
| 11       | IRQ3  | 1          | Serial Port 2, Expansion Bus B25                  |
| 12       | IRQ4  | 1          | Serial Port 1, Expansion Bus B24                  |
| 13       | IRQ5  | 1          | Parallel Port 2, Expansion Bus B23                |
| 14       | IRQ6  | 1          | Diskette Controller, Expansion Bus B22            |
| 15       | IRQ7  | 1          | Parallel Port 1, Expansion Bus B21                |

The following demonstrates the interrupt sequence for a 80x86-type system.

1. One or more of the Interrupt Request (IRQ[x]) lines are raised high, setting the corresponding Interrupt Request Register (IRR) bit(s).
2. The Interrupt Controller evaluates these requests, and sends an INTR to the CPU, if appropriate.
3. The CPU acknowledges the INTR and responds with an interrupt acknowledge cycle. This cycle is translated

into a PCI bus command. This PCI command is broadcast over the PCI bus as a single cycle.

4. Upon receiving an interrupt acknowledge cycle from the CPU over the PCI, the PCI-EISA bridge (PCEB) converts the single cycle into an INTA# pulse to the ESC. The ESC uses the INTA# pulse to generate the two cycles that the internal 82C59 pair can respond to with the expected interrupt vector. The cycle conversion is performed by a functional block in the ESC Interrupt Controller Unit.

10 The internally generated interrupt acknowledge cycle is completed as soon as possible as the PCI bus is held in wait states until the interrupt vector data is returned.

Each cycle appears as an interrupt acknowledge pulse on the INTA# pin of the cascaded interrupt controllers.

These two pulses are not observable at the ESC periphery.

5. Upon receiving the first internally generated interrupt acknowledge, the highest priority In-Service Register (ISR) bit is set and the corresponding IRR bit is reset.

20 The Interrupt Controller does not drive the Data Bus during this cycle. On the trailing edge of the first cycle pulse, a slave identification code is broadcast by the master to the slave on a private, internal three bit wide bus. The slave controller uses these bits to

determine if it must respond with an interrupt vector during the second INTA# cycle.

6. Upon receiving the second internally generated interrupt acknowledge, the Interrupt Controller releases an 8 bit pointer (the interrupt vector) onto the Data Bus where it is read by the CPU.

7. This generally completes the interrupt cycle. In an automatic end-of-interrupt mode the ISR bit is reset at the end of the second interrupt acknowledge cycle pulse. Otherwise, the ISR bit remains set until an appropriate end-of-interrupt (EOI) command is issued at the end of the interrupt subroutine.

At the system level, the APIC consists of two parts -- one residing in the I/O subsystem (I/O APIC 420) and the other, local APIC 120, 220, and 320, residing in processor 110, processor 210, and processor 310, respectively. The local APIC and I/O APIC 420 communicate over dedicated APIC bus 400. The ESC's I/O APIC bus interface consists of bi-directional data signals and a clock input. Each local APIC (local APIC 120, local APIC 220, and local APIC 320) contains intelligence to determine whether or not each processor should accept interrupts broadcast on APIC bus 400. The local APIC unit also provides local pending of interrupts, nesting and masking of interrupts, and handles all interactions with its local processor (e.g.,

interrupt request (INTR), interrupt acknowledge (INTA, and EOI protocol). Each local APIC also provides inter-processor interrupts and a timer to its local processor.

As shown in **Figure 2**, the invention contemplates  
5 identifying and redirecting EISA compatible interrupt signals (block 450), masking the EISA compatible interrupt controller interrupt addresses (block 460) and re-directing the interrupt addresses to the I/O APIC (block 470). In this manner, some or all of the interrupts handled by the EISA compatible interrupt controller (e.g., the 82C59 controller(s)) are instead handled  
10 by the I/O APIC.

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**Figure 3** describes a method of redirecting 82C59 interrupt addresses to an I/O APIC. This embodiment takes advantage of the normal process of initializing interrupt registers on system start-up. The embodiment seeks to identify 82C59 interrupt addresses through system logic. One way this is accomplished is by configuring a system management interrupt (SMI) to trap a configuring 82C59 address (block 510). An SMI is derived from power management architecture of the ESC. In particular, the system management mode (SMM) is a function of the ESC's power management architecture that includes software that controls transitions between a Power-On state and a Fast-Off state. The Fast-Off state is generally utilized in modern processors to permit a system to operate in a low power state without being

powered down. When the system is in a Fast-Off state, the system consumes less power than the Power-On state and is not in a Power Off state. Events such as pressing a key on a keyboard or moving a mouse constitutes a Fast-On event to convert from a

5 Fast-Off state to a Power-On state.

To invoke SMM software, the ESC generates an SMI to the processor. An SMI offers serialized execution. Once an SMI happens, the processor stops and processes the SMI.

The 82C59 generally contains four initializing address  
10 registers -- 20h, 21h, A0h, A1h. The four address registers are initialized by four initialization command words: ICW1, ICW2,  
ICW3, and ICW4. Before normal operation can begin, each interrupt controller in the system must be initialized. In the  
ESC, this is a four byte sequence. The base address for each  
15 interrupt controller is a fixed location in I/O memory space, at 0020h for CNTRL-1 and 00A0h for CNTRL-2. An I/O write to the  
CNTRL-1 or CNTRL-2 base address with data bit 4 equal to 1 is interpreted as ICW1. For ESC-based EISA systems, three I/O  
writes to "base address + 1" (021h for CNTRL-1 and 0A0h for  
20 CNTRL-2) must follow the ICW1. The first write to "base address  
+ 1" (021h/0A0h) performs ICW2, the second write performs ICW3,  
and the third write performs ICW4. Initialization of the 82C59 controller thus generally occurs in a particular sequence, ICW1,  
ICW2, ICW3, and ICW4.

In one embodiment, an SMI is configured to recognize and trap a configuring 82C59 address, such as one of the identified initialization command words. In addition to trapping a configuring 82C59 address, the trapped address is analyzed to determine whether or not the address is the first configuring address (block 520). As noted above, 82C59 is configured in a specific sequence, therefore, prior to re-routing the initialization addresses to I/O APIC as a trap, the SMI locates the first configuring address. A look-up table containing the appropriate order of the initialization command words is provided to identify the appropriate configuring address.

1000 999 998 997 996 995 994 993 992 991 990 989 988 987 986 985 984 983 982 981 980 979 978 977 976 975 974 973 972 971 970 969 968 967 966 965 964 963 962 961 960 959 958 957 956 955 954 953 952 951 950 949 948 947 946 945 944 943 942 941 940 939 938 937 936 935 934 933 932 931 930 929 928 927 926 925 924 923 922 921 920 919 918 917 916 915 914 913 912 911 910 909 908 907 906 905 904 903 902 901 900 899 898 897 896 895 894 893 892 891 890 889 888 887 886 885 884 883 882 881 880 879 878 877 876 875 874 873 872 871 870 869 868 867 866 865 864 863 862 861 860 859 858 857 856 855 854 853 852 851 850 849 848 847 846 845 844 843 842 841 840 839 838 837 836 835 834 833 832 831 830 829 828 827 826 825 824 823 822 821 820 819 818 817 816 815 814 813 812 811 810 809 808 807 806 805 804 803 802 801 800 799 798 797 796 795 794 793 792 791 790 789 788 787 786 785 784 783 782 781 780 779 778 777 776 775 774 773 772 771 770 769 768 767 766 765 764 763 762 761 760 759 758 757 756 755 754 753 752 751 750 749 748 747 746 745 744 743 742 741 740 739 738 737 736 735 734 733 732 731 730 729 728 727 726 725 724 723 722 721 720 719 718 717 716 715 714 713 712 711 710 709 708 707 706 705 704 703 702 701 700 699 698 697 696 695 694 693 692 691 690 690 689 688 687 686 685 684 683 682 681 680 680 679 678 677 676 675 674 673 672 671 670 670 669 668 667 666 665 664 663 662 661 660 660 659 658 657 656 655 654 653 652 651 650 650 649 648 647 646 645 644 643 642 641 640 640 639 638 637 636 635 634 633 632 631 630 630 629 628 627 626 625 624 623 622 621 620 620 619 618 617 616 615 614 613 612 611 610 610 609 608 607 606 605 604 603 602 601 600 599 598 597 596 595 594 593 592 591 590 590 589 588 587 586 585 584 583 582 581 580 580 579 578 577 576 575 574 573 572 571 570 570 569 568 567 566 565 564 563 562 561 560 560 559 558 557 556 555 554 553 552 551 550 550 549 548 547 546 545 544 543 542 541 540 540 539 538 537 536 535 534 533 532 531 530 530 529 528 527 526 525 524 523 522 521 520 520 519 518 517 516 515 514 513 512 511 510 510 509 508 507 506 505 504 503 502 501 500 499 498 497 496 495 494 493 492 491 490 490 489 488 487 486 485 484 483 482 481 480 480 479 478 477 476 475 474 473 472 471 470 470 469 468 467 466 465 464 463 462 461 460 460 459 458 457 456 455 454 453 452 451 450 450 449 448 447 446 445 444 443 442 441 440 440 439 438 437 436 435 434 433 432 431 430 430 429 428 427 426 425 424 423 422 421 420 420 419 418 417 416 415 414 413 412 411 410 410 409 408 407 406 405 404 403 402 401 400 399 398 397 396 395 394 393 392 391 390 390 389 388 387 386 385 384 383 382 381 380 380 379 378 377 376 375 374 373 372 371 370 370 369 368 367 366 365 364 363 362 361 360 360 359 358 357 356 355 354 353 352 351 350 350 349 348 347 346 345 344 343 342 341 340 340 339 338 337 336 335 334 333 332 331 330 330 329 328 327 326 325 324 323 322 321 320 320 319 318 317 316 315 314 313 312 311 310 310 309 308 307 306 305 304 303 302 301 300 299 298 297 296 295 294 293 292 291 290 290 289 288 287 286 285 284 283 282 281 280 280 279 278 277 276 275 274 273 272 271 270 270 269 268 267 266 265 264 263 262 261 260 260 259 258 257 256 255 254 253 252 251 250 250 249 248 247 246 245 244 243 242 241 240 240 239 238 237 236 235 234 233 232 231 230 230 229 228 227 226 225 224 223 222 221 220 220 219 218 217 216 215 214 213 212 211 210 210 209 208 207 206 205 204 203 202 201 200 200 199 198 197 196 195 194 193 192 191 190 190 189 188 187 186 185 184 183 182 181 180 180 179 178 177 176 175 174 173 172 171 170 170 169 168 167 166 165 164 163 162 161 160 160 159 158 157 156 155 154 153 152 151 150 150 149 148 147 146 145 144 143 142 141 140 140 139 138 137 136 135 134 133 132 131 130 130 129 128 127 126 125 124 123 122 121 120 120 119 118 117 116 115 114 113 112 111 110 110 109 108 107 106 105 104 103 102 101 100 100 99 98 97 96 95 94 93 92 91 90 90 89 88 87 86 85 84 83 82 81 80 80 79 78 77 76 75 74 73 72 71 70 70 69 68 67 66 65 64 63 62 61 60 60 59 58 57 56 55 54 53 52 51 50 50 49 48 47 46 45 44 43 42 41 40 40 39 38 37 36 35 34 33 32 31 30 30 29 28 27 26 25 24 23 22 21 20 20 19 18 17 16 15 14 13 12 11 10 10 9 8 7 6 5 4 3 2 1 0

Once the SMI locates the first configuring address, the SMI then locates the remaining configuring addresses (block 530). An SMI vector handler is then generated to direct the appropriate processor to find the interrupt (block 540). The SMI vector handler is associated with the I/O APIC. Once the SMI vector handler is generated, an SMI vector is passed to the appropriate processor (block 550). In response to the SMI vector, the processor re-routes configuring addresses to the I/O APIC (block 560). In this regard, the I/O APIC is then configured to handle 82C59 interrupts.

By handling all 82C59 interrupts through the APIC system, the invention supports the use of conventional chip set systems with advanced operating systems that do not support 82C59

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interrupt control. The invention also supports the use of such chip set systems in multi-processor environments.

In the preceding detailed description, the invention is described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

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CLAIMS

What is claimed is:

1 1. A method comprising:  
2 trapping initializing data of a first interrupt type to a  
3 first interrupt controller;  
4 re-routing the initializing data of the first interrupt  
5 type to a second interrupt controller; and  
6 configuring the second interrupt controller to manage  
7 interrupts of the first interrupt type.

1 2. The method of claim 1, wherein trapping initializing data  
2 of a first interrupt type comprises:  
3 configuring a system management interrupt to recognize  
4 initializing data of a first interrupt type.

1 3. The method of claim 1, wherein initializing data of the  
2 first interrupt type comprises a plurality of command words and  
3 a first command word begins the initializing of the first  
4 interrupt controller, configuring a system management interrupt  
5 to recognize initializing data of a first interrupt type and re-  
6 route initializing data to the second interrupt controller from  
7 the first command word.

1   4.   The method of claim 1, wherein the first interrupt  
2 controller comprises an 82C59 controller and the second  
3 interrupt controller comprises a advanced programmable interrupt  
4 controller.

1   5.   A machine readable storage media containing executable  
2 program instructions which when executed cause a digital  
3 processing system to perform a method comprising:

4                 trapping initializing data of a first interrupt type to a  
5 first interrupt controller;

6                 re-routing initializing data of a first interrupt type to a  
7 second interrupt controller; and

8                 configuring the second interrupt controller to manage  
9 interrupts of the first interrupt type.

1   6.   The media of claim 5, wherein trapping initializing data of  
2 a first interrupt type comprises:

3                 configuring a system management interrupt to recognize  
4 initializing data of a first interrupt type.

1   7.   The media of claim 5, wherein initializing data of the  
2 first interrupt type comprises a plurality of command words and  
3 a first command word begins the initializing of the first

4 interrupt controller, configuring a system management interrupt  
5 to recognize initializing data of a first interrupt type and re-  
6 route initializing data to the second interrupt controller from  
7 the first command word.

1 8. The media of claim 5, wherein the first interrupt  
2 controller comprises an 82C59 controller and the second  
3 interrupt controller comprises a advanced programmable interrupt  
4 controller.

1 9. A system comprising:  
2       a central processing unit (CPU);  
3       a first bus coupled to the CPU;  
4       a first interrupt controller, coupled to the first bus,  
5 operable to manage communication with the CPU of interrupts of a  
6 first interrupt type;  
7       a second bus coupled to the CPU;  
8       a second interrupt controller, coupled to the second bus  
9 and to the first interrupt controller, operable to manage  
10 communication with the CPU of interrupts of a second interrupt  
11 type; and  
12       a memory coupled to the second interrupt controller  
13 comprising a computer-readable medium having a computer-readable

14 program embodied therein for directing operation of the system,  
15 the computer-readable program comprising:  
16       instructions for managing interrupts of the first interrupt  
17 type by the second interrupt controller.

1 10. The system of claim 9, wherein the computer-readable  
2 program further comprises:

3       instructions for trapping initializing data of a first  
4 interrupt type to the first interrupt controller;

5       instructions for re-routing initializing data of a first  
6 interrupt type to the second interrupt controller; and

7       instructions for configuring the second interrupt  
8 controller to manage interrupts of the first interrupt type.

1 11. The system of claim 10, wherein the instructions for  
2 trapping initializing data comprise:

3       instructions for configuring a system management interrupt  
4 to recognize initializing data of a first interrupt type.

1 12. The system of claim 10, wherein initializing data of the  
2 first interrupt type comprise a plurality of command words and a  
3 first command word begins the initializing of the first  
4 interrupt controller, and the computer-readable program  
5 comprises instructions for configuring a system management

6 interrupt to recognize initializing data of a first interrupt  
7 type and re-route initializing data to the second interrupt  
8 controller from the first command word.

1 13. The system of claim 9, wherein the first interrupt  
2 controller comprises an 82C59 controller and the second  
3 interrupt controller comprises a advanced programmable interrupt  
4 controller.

1 14. The system of claim 13, wherein the second interrupt  
2 controller manages interrupts of the first interrupt type  
3 exclusive of the first interrupt controller.

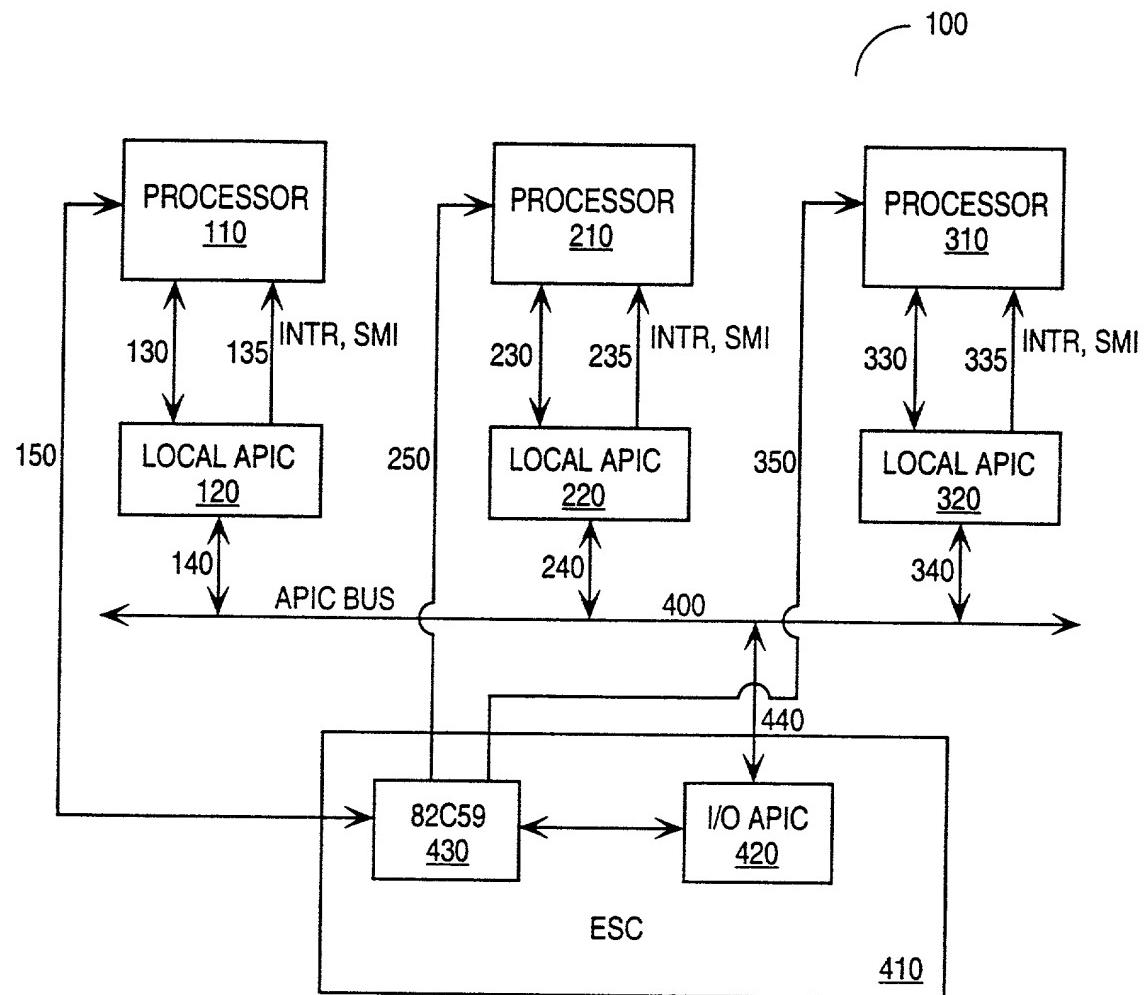
1 15. A system comprising:  
2       a central processing unit (CPU);  
3       first means of interrupt processing for managing  
4 communication with the CPU of interrupts of a first interrupt  
5 type;  
6       second means of interrupt processing for managing  
7 communication with the CPU of interrupts of a second interrupt  
8 type;  
9       means for routing interrupts of the first interrupt type to  
10 the second interrupt processing means

11 means for managing interrupts of the first interrupt type  
12 by the second interrupt processing means exclusive of the first  
13 interrupt processing means.

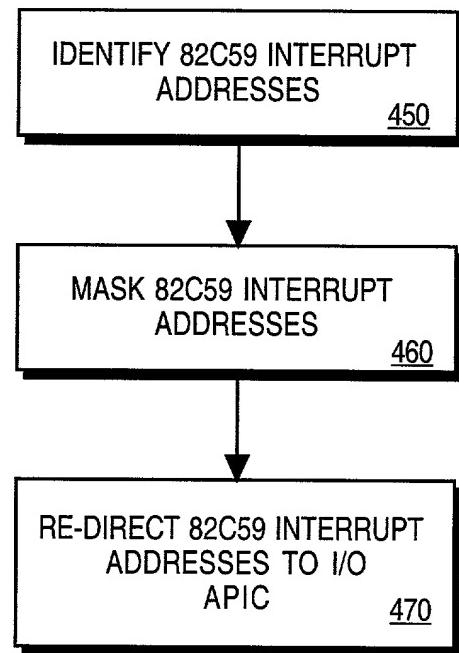
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## **ABSTRACT**

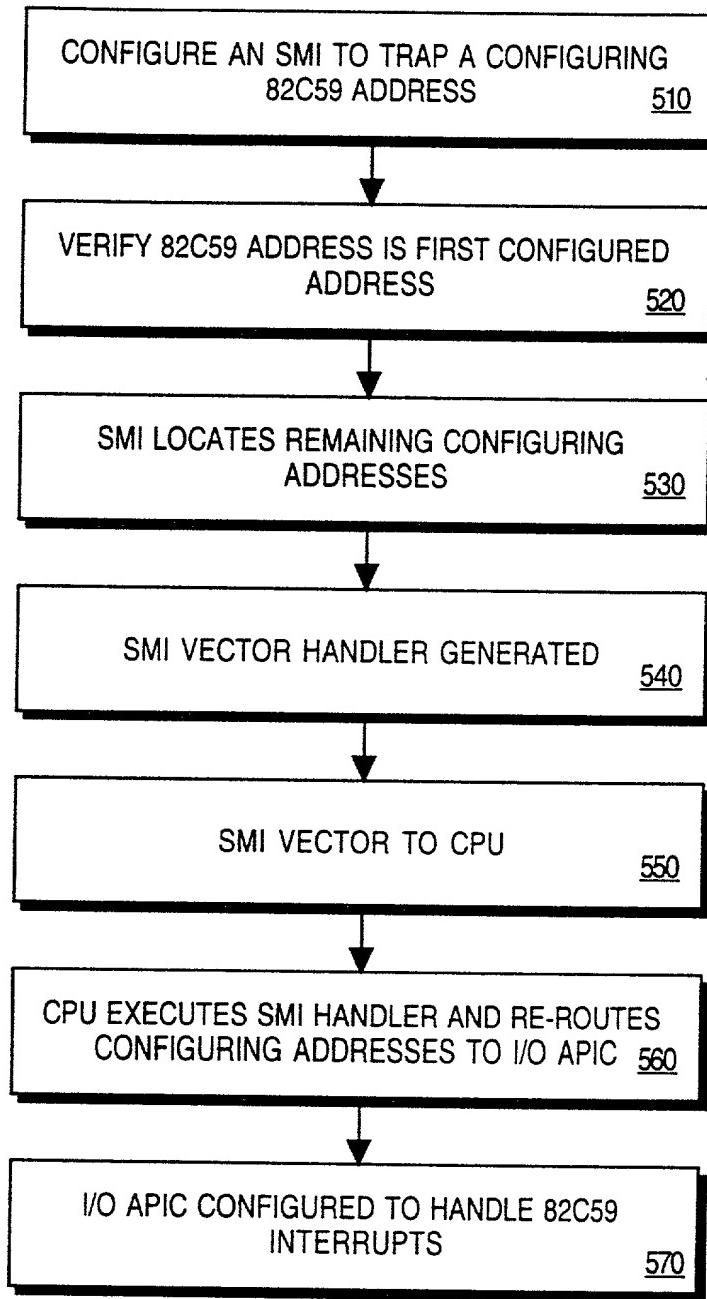
In one aspect, a method is disclosed. The method includes trapping initializing data of a first interrupt type to a first interrupt controller, re-routing the initializing data of the first interrupt type to a second interrupt controller, and configuring the second interrupt controller to manage interrupt of the first interrupt type.



**FIG. 1**



**FIG. 2**



**FIG. 3**